REMARKS

This application has been reviewed in light of the Office Action dated November 3, 2005. Claims 1-16 and 32-35 are pending in the application. By the present amendment, claims 1 and 9 have been amended. Claims 17-31 have been canceled without prejudice. The Applicant reserves the right to pursue claims 17-31 by a separate divisional filing. Claims 32-35 have been introduced. No new matter has been added. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

By the Office Action, claims 1-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa et al. (NPL reference "U", hereinafter Ogawa) in view of Huston et al. (NPL Reference "V", hereinafter Huston).

Ogawa is directed to a study of stress induced voids (SIV) for Cu metallization in integrated circuits. Ogawa is concerned with mass migration due to stress. Ogawa states that dual damascene structures are the "weak-link" in the chain of interconnections, and uses the dual damascene structure to test the effects of void formation due to stress in this dual damascene structure. The structures underwent a 7-level metal process flow and were then subjected to a 500 hour bake to induce grain growth. The 500 hour bake process would not be employed in fabricating a semiconductor chip.

The scientific research conducted by Ogawa fails to disclose or suggest anything about device yield or its effect on the reliability of a semiconductor chip structure. Instead, Ogawa sets forth a procedure for attempting to grow micro voids in Cu to study and characterize their growth relative to Al structures. Ogawa is attempting to determine if Cu

metallizations pose a micro void risk. One skilled in the art reading Ogawa would not know how to apply the teachings of Ogawa to arrive at the present invention or to combine the teachings of Ogawa with Huston to arrive at the present claims.

Although, Ogawa employs a similar dual damascene structure, the structure is created and processed to create void growth under conditions to characterize the void growth itself. This data is not specific to a semiconductor device nor is this data used to determine a semiconductor device's reliability.

Huston provides a mathematical relationship between yield and reliability, but fails to cure the deficiencies of Ogawa. Huston creates yield and reliability models to attempt to link the two and determine under which conditions the two models can be linked. There is no suggestion that the yield of a test structure be used to determine the reliability of a semiconductor structure made by the same process.

The present invention builds a test structure, applies thermal changes and measures the yield of the test structure. Then, the yield of the test structure is employed to determine reliability for the actual semiconductor device/structure. The yield of the semiconductor structure is associated with the yield of the test structure, even though the actual yield of the semiconductor structure is not known. There is no disclosure or suggestion in the cited references that discloses these concepts.

Claim 1 includes, *inter alia*, a method for evaluating reliability of a semiconductor chip structure built by a manufacturing process including building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure; thermal cycling the test

structure; measuring a yield of the test structure; and evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield of the test structure.

The cited references fail to disclose or suggest at least:

1) building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure; and

2) evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield of the test structure.

Claim 1 was amended to further clarify these distinctions. Claim 9 has also been amended in a similar manner as claim 1. Since Ogawa and/or Huston fail to disclose or suggest any of the previously described aspects of the present invention, claims 1 and 9 are believed to be in condition for allowance for at least the reasons stated. Claims 2-8 and 10-16 are also believed to be in condition for allowance due at least to their dependencies from claim 1 and 9, respectively. Other reasons exist for allowing the dependent claims.

For example, claims 3 and 12 include fabricating the test structure to provide a uniform stress condition on one or more structures. This is not disclosed in Ogawa which suggests that there are high stress regions of concern, which may cause mass migration issues in the dual damascene structure. Further, FIG. 8 of Ogawa shows different stress levels in the structure.

Claims 7 and 15 recite that the step of building includes building the test structure to provide a bimodal failure distribution having early and late fails during thermal

cycle testing, and claims 8 and 16 recite that the step of evaluating reliability is based on early fails. These aspects are not disclosed or suggested by the cited combination.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

Date: 2/3/06

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